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[LY62256PL-55LLI](#)

[LY62256SL-55LLI](#)

[LY62256SL-70LL](#)

EN

This Datasheet is presented by
the manufacturer

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Hersteller bereitgestellt

FR

Cette fiche technique est
présentée par le fabricant



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0.	Initial Issue	Jul.25.2004
Rev. 2.0.	Revised Vcc Range(Vcc=4.5~5.5V => 2.7~5.5V)	May.4.2005
Rev. 2.1.	Revised I _{SB1}	May.13.2005
Rev. 2.2	Adding PKG type : skinny P-DIP	Aug.29.2005
Rev. 2.3	Revised V _{IH} (min)=2.4V, V _{IL} (max)=0.6V	Feb.24.2006
Rev. 2.4	Revised V _{IH} (min)=2.4V, V _{IL} (max)=0.6V (V _{CC} =2.7~3.6V) V _{IH} (min)=2.4V, V _{IL} (max)=0.8V (V _{CC} =4.5~5.5V)	Jul.31.2006
Rev. 2.5	Revised STSOP Package Outline Dimension	Mar.26.2008
Rev. 2.6	Added SL grade Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Revised I _{SB1} (MAX) Revised V _{TERM} to V _{T1} and V _{T2} Revised Test Condition of I _{SB1} /I _{DR} Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS	Mar.30.2009
Rev. 2.7	Revised PACKAGE OUTLINE DIMENSION in page 8 & 9	Dec.18.2009
Rev. 2.8	Revised PACKAGE OUTLINE DIMENSION in page 10	May.7.2010
Rev. 2.9	Revised ORDERING INFORMATION in page 12 Revised PACKAGE OUTLINE DIMENSION in page 9	Aug.25.2010

FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:
Operating current : 20/15/10mA (TYP.)
Standby current : 1μA (TYP.)
- Single 2.7~5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 600 mil PDIP
28-pin 330 mil SOP
28-pin 8mm x 13.4mm STSOP
28-pin 300 mil Skinny P-DIP

GENERAL DESCRIPTION

The LY62256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

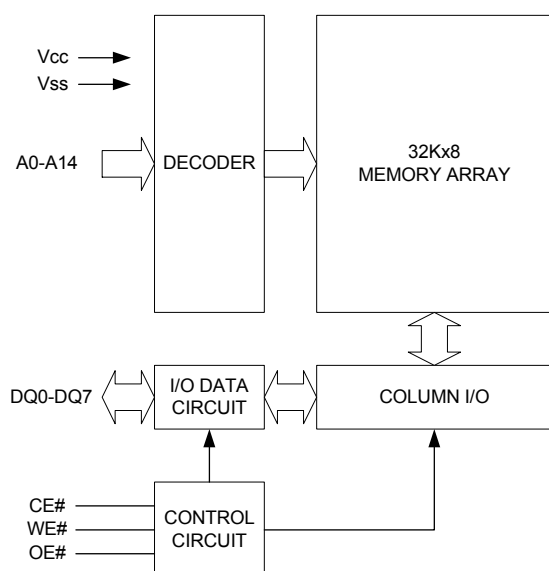
The LY62256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62256 operates from a single power supply of 2.7~5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY62256	0 ~ 70°C	2.7 ~ 5.5V	35/55/70ns	1μA	20/15/10mA
LY62256(E)	-20 ~ 80°C	2.7 ~ 5.5V	35/55/70ns	1μA	20/15/10mA
LY62256(I)	-40 ~ 85°C	2.7 ~ 5.5V	35/55/70ns	1μA	20/15/10mA

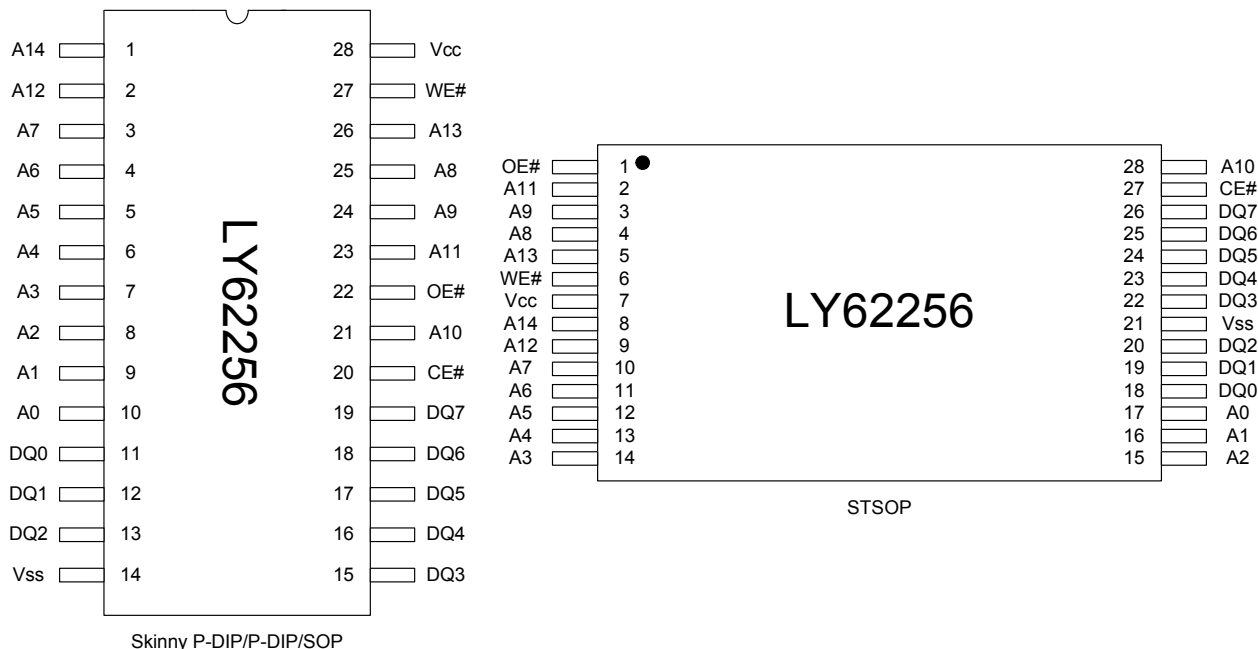
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



Skinny P-DIP/P-DIP/SOP

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}		2.7	3.3	5.5	V
Input High Voltage	V _{IH} ^{*1}		2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}	V _{CC} =2.7~3.6V	- 0.5	-	0.6	V
		V _{CC} =4.5~5.5V	- 0.5	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	3.0	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min.	-35	20	50	mA
		CE# = V _{IL} , I _{I/O} = 0mA	-55	15	45	mA
		Other pins at V _{IL} or V _{IH}	-70	10	40	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	3	10	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , other pins at V _{IL} or V _{IH}	-	1	3	mA
	I _{SB1}	CE# ≥ V _{CC} -0.2V Others at 0.2V or V _{CC} - 0.2V	LL	1	20	μA
			LLE/LLI	1	30	μA
			SL ^{*5} 25°C	1	3	μA
			SLE ^{*5} 40°C	1.5	4	μA
			SLI ^{*5}	1.5	4	μA
			SL	1	10	μA
			SLE/SLI	1	20	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 50pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62256-35		LY62256-55		LY62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	ns

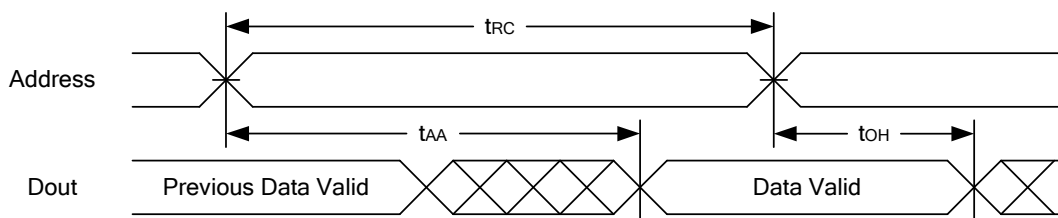
(2) WRITE CYCLE

PARAMETER	SYM.	LY62256-35		LY62256-55		LY62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	-	25	ns

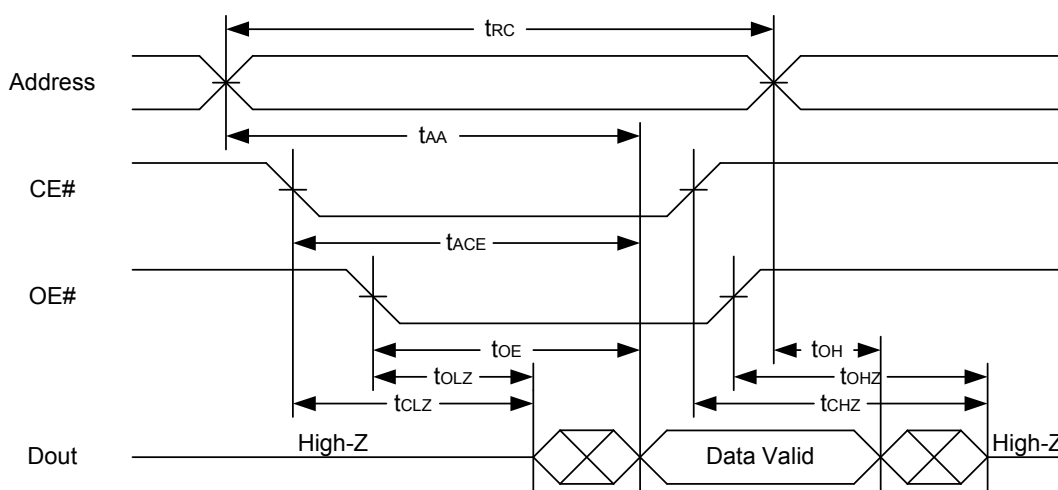
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



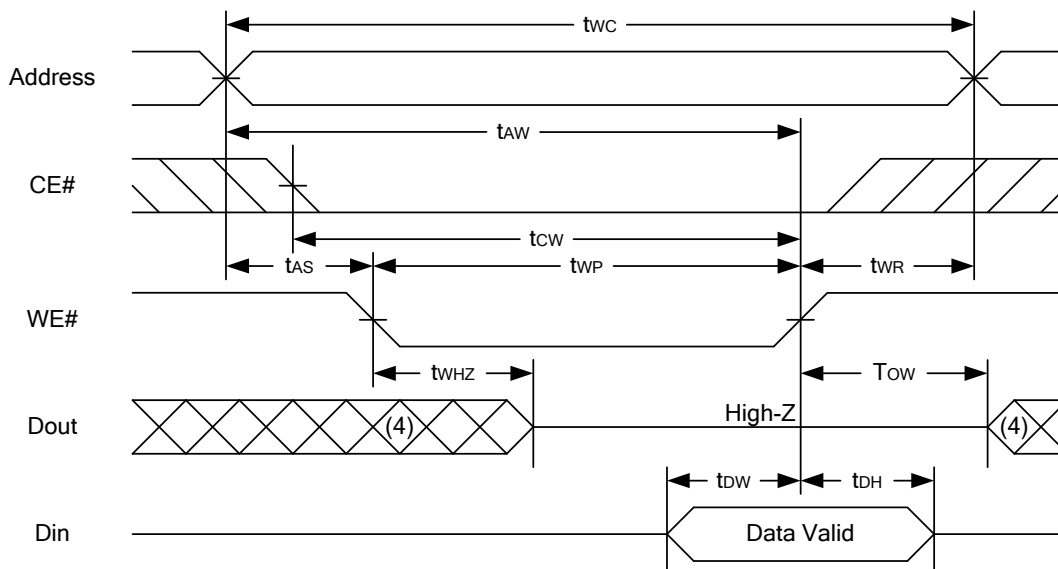
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



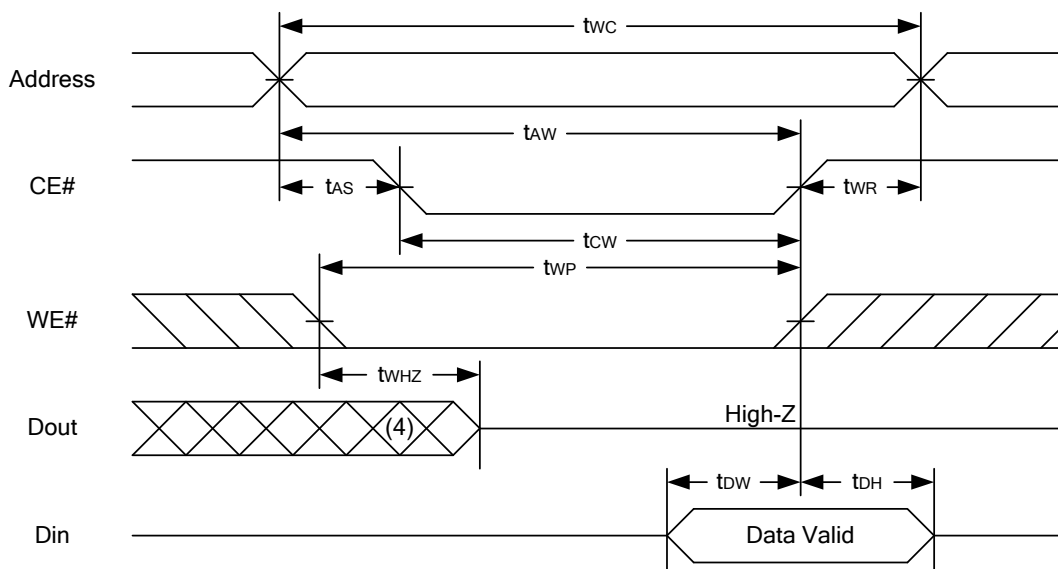
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

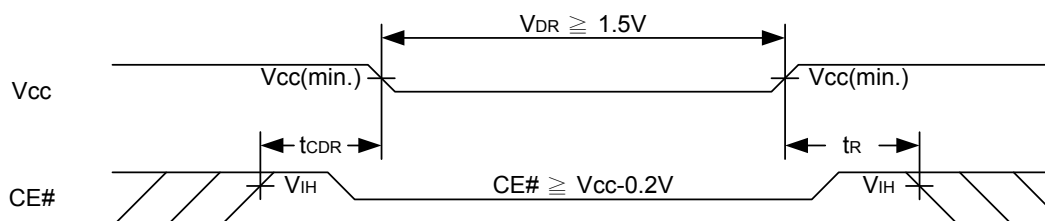
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, twp must be greater than twhZ + tDQ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V			1.5	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	LL/LLE/LLI		-	0.5	20	μA
			SL	25°C	-	0.5	2	μA
			SLE	40°C	-	1	3	μA
			SLI		-			μA
			SL		-	0.5	8	μA
			SLE/SLI	-	0.5	15	μA	
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t _R				t _{RC} *	-	-	ns

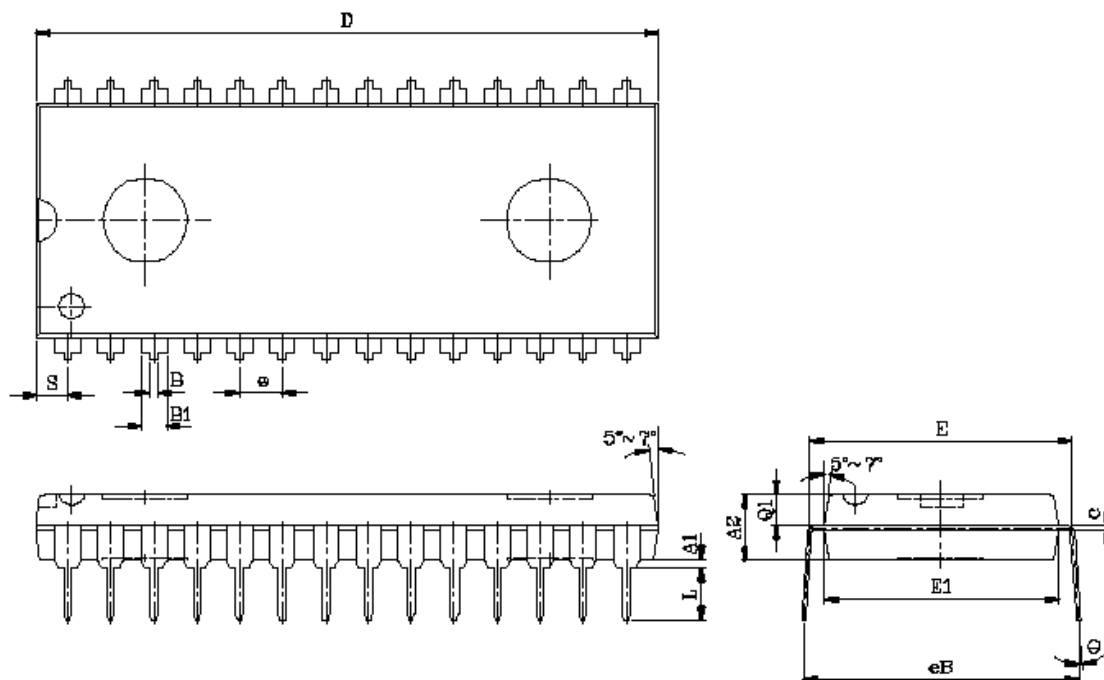
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



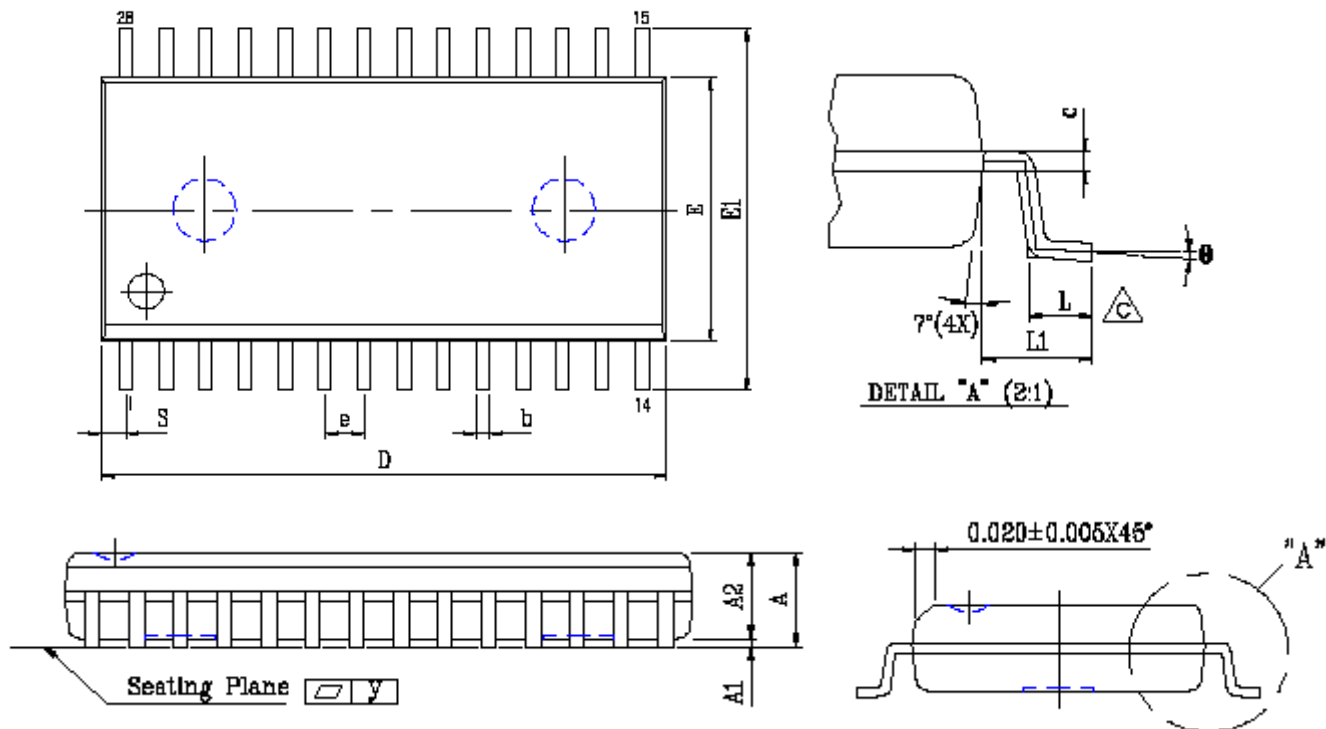
PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension

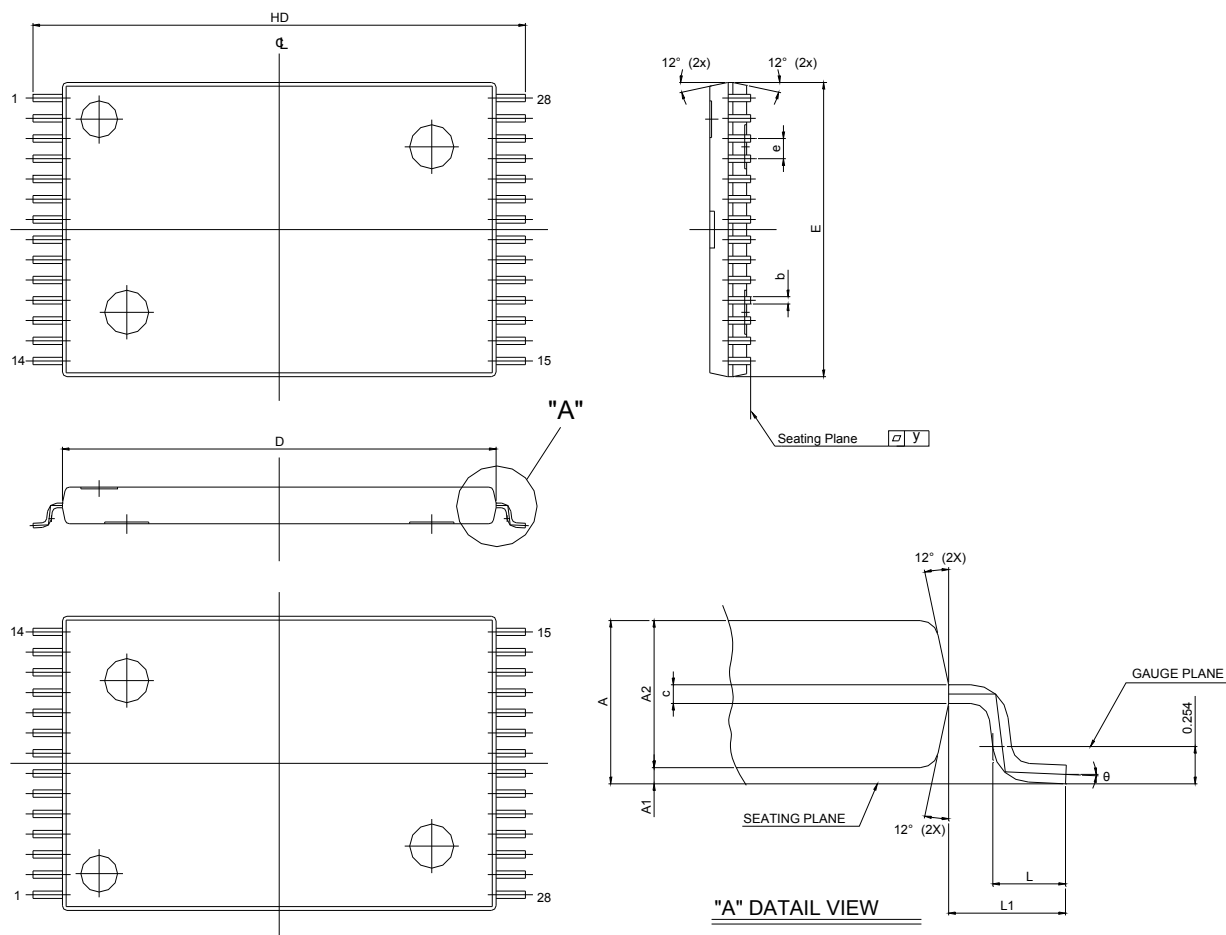


SYM.	UNIT	INCH.(BASE)	MM(REF)
A1		0.015(MIN)	0.381(MIN)
A2		0.155±0.005	3.937±0.127
B		0.020(MAX)	0.508(MAX)
B1		0.060(TYP)	1.524(TYP)
c		0.012(MAX)	0.304(MAX)
D		1.470(MAX)	37.338(MAX)
E		0.6(TYP)	15.24(TYP)
E1		0.55(MAX)	13.970(MAX)
e		0.100(TYP)	2.540(TYP)
eB		0.650±0.020	16.510±0.508
L		0.200(MAX)	5.080(MAX)
S		0.06(MAX)	1.524(MAX)
Q1		0.08(MAX)	2.032(MAX)
Θ		15°(MAX)	15°(MAX)

28 pin 330 mil SOP Package Outline Dimension

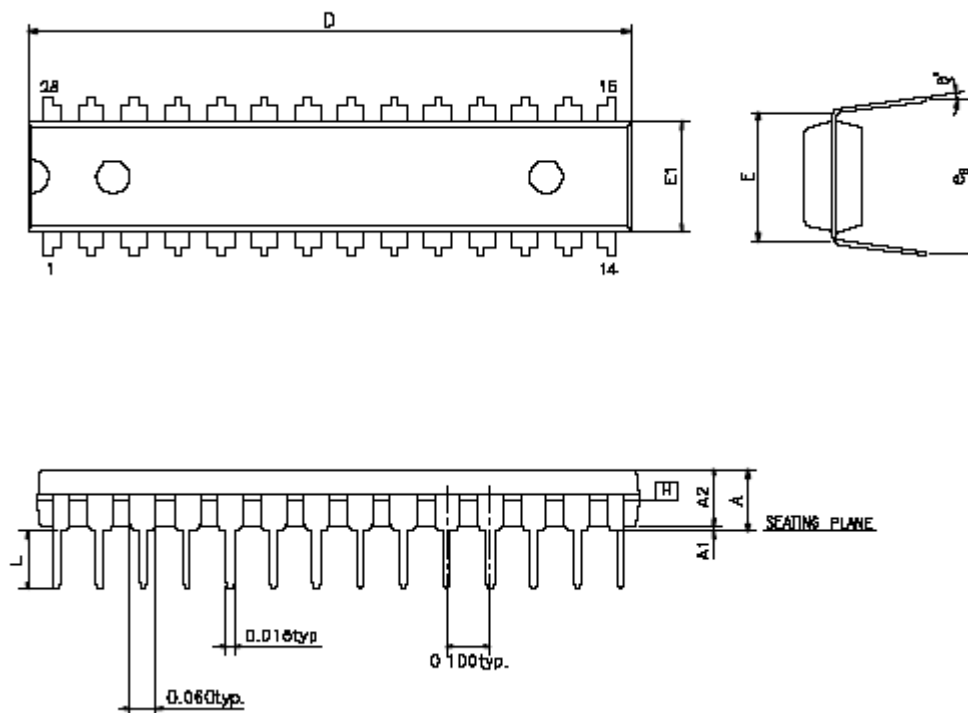


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098±0.005	2.489±0.127
b		0.016(TYP)	0.406(TYP)
c		0.010(TYP)	0.254(TYP)
D		0.728(MAX)	18.491(MAX)
E		0.340(MAX)	8.636(MAX)
E1		0.465±0.012	11.811±0.305
e		0.050(TYP)	1.270(TYP)
L		0.038(MAX)	0.965(MAX)
L1		0.067±0.008	1.702 ±0.203
S		0.047(MAX)	1.194(MAX)
y		0.004(MAX)	0.102(MAX)
Θ		0°~10°	0°~10°

28 pin 8x13.4mm STSOP Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°

28 pin 300 mil PDIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
eB	0.330	0.350	0.370
θ*	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH



ORDERING INFORMATION

LY62256 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray

Tube : 28-pin 600 mil P-DIP

28-pin 330 mil SOP

28-pin 300 mil P-DIP

Tray : 28-pin 8 mm x 13.4 mm STSOP

T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C

E : (Extended) -20°C ~ +80°C

I : (Industrial) -40°C ~ +85°C

XX : Power Type

LL : Ultra Low Power

SL : Special Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

P : 28-pin 600 mil P-DIP

S : 28-pin 330 mil SOP

R : 28-pin 8 mm x 13.4 mm STSOP

D : 28-pin 300 mil P-DIP



Lyontek Inc.

LY62256

Rev. 2.9

32K X 8 BIT LOW POWER CMOS SRAM

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